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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/674,984	01/08/2001	Volker Becker	10191/1565	9242

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KENYON & KENYON
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/674,984	BECKER ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on th cov r sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43-48* is/are allowed.

6)☒ Claim(s) *23-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 29, 2004 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 23-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blayo et al., U.S. Patent 5,739,909 as applied to claims 23-30 and 37 above, and further in view of Abidi et al., U.S. Patent 5,539,241.

2. Pertaining to claim 23, Blayo discloses a semiconductor device substantially as claimed. See **FIGS. 1 & 2**, where Blayo teaches a device for determining an extent of an at least locally undercut of a structured surface layer on a sacrificial layer, comprising:

at least one passive electronic component **40**(column 1, line 14, semiconductor device) arranged on a the structured surface layer for determining a physical measured quantity that is proportional to the extent of the lateral undercut on a sacrificial layer(column 1, lines 23-34).

However, Blayo fails to discloses the passive electronic device in the shape of a coil, the at least one passive electronic component configured to determine a physical a physical measured quantity. Abidi discloses a passive electronic device in the shape of a coil. In view of Abidi, it would have been obvious to one of ordinary skill in the art to incorporate a passive electronic device in a shape of a coil in the Blayo semiconductor device, because the coil has a self resonant frequency (see Abstract).

3. Pertaining to claim 24, Blayo teaches wherein the physical measured quantity corresponds to one of:

a capacitance,

one of an absorbed intensity and an emitted intensity of an electromagnetic emission,

one of an absorbed frequency and an emitted frequency, and

one of an absorbed frequency spectrum and an emitted frequency spectrum of the electromagnetic emission.

4. Pertaining to claim 25, Blayo teaches wherein the one of the absorbed frequency and the emitted frequency corresponds to a resonance frequency.

5. Pertaining to claim 26, Blayo teaches wherein at least one transmitter **20** for emitting a first signal;

at least one receiver **60** for detecting a second signal, the at least one passive electronic component **40** interacting with the first signal and one of generating the second signal and transforming the first signal into the second signal.

6. Pertaining to claim 27, Blayo teaches wherein the physical measured quantity is determined from one of:

the second signal, and

a difference between the first signal and the second signal and the second signal.

7. Pertaining to claim 28, Blayo, teaches wherein the at least one transmitter and the at least one receiver are integrated in an assembly.

8. Pertaining to claim 29, Blayo teaches wherein the assembly includes a processing unit.

9. Pertaining to claim 30, Blayo teaches wherein the at least one transmitter is at the same time also the at least one receiver.

10. Pertaining to claim 37, Blayo teaches wherein the structured surface layer, at least in an area of the at least one passive electronic component, is separated from a base layer by the sacrificial layer.

11. Blayo discloses a semiconductor device substantially as claimed as discussed above, however, Blayo fails to teach the following limitations.

Pertaining to claims 33, 35 and 37, Blayo fails to teach wherein the coil delineated out in the structure surface layer and including a firs coil end and a second coil end, the coil and a base layer arranged with respect to the structured surface layer and the sacrificial layer form a capacitor having a capacitance proportional to the extent of the lateral undercut. Abidi teaches a passive electron component which includes a coil delineated out in the structure surface layer

and including a firs coil end and a second coil end, the coil and a base layer arranged with respect to the structured surface layer and the sacrificial layer form a capacitor having a capacitance proportional to the extent of the lateral undercut. See **FIGS. 2** and **4a**, where Abidi teaches an inductor having a built in capacitor (parasitic capacitor). In view of Abidi, it would have been obvious to one of ordinary skill in the art to incorporate the passive component of Abidi into the Blayo semiconductor device because there are numerous advantages to integrating not only the transistor but also the inductors and other passive components because manufacturing cost and power consumption can be substantially reduced (column 1, lines 13-17). Please note that the passive electronic component is separated from a base layer by the sacrificial layer.

12. Pertaining to claims 36, Blayo fails to teach wherein at least one of the first coil end is dimensioned in an extent thereof such that a complete undercut of the at least one of the first coil end and the second coil end does not occur. Abidi teaches wherein at least one of the first coil end is dimensioned in an extent thereof such that a complete undercut of the at least one of the first coil end and the second coil end does not occur. See **FIG. 2** of Abidi where the coil ends are not undercut. In view of Abidi, it would have been obvious to one of ordinary skill in the art to not undercut the coil ends in the Blayo semiconductor device because the motivation is to provide a stable platform for the coil ends.

13. Claims 38, 39, 40, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blayo et al., U.S. Patent 5,739,909 in view of Abidi et al., U.S. Patent 5,539,241 as applied to claims 23-30, 33, 35, 36 and 37 above, and further in view of Curran, U.S. Patent 5,126,284.

14. Pertaining to claims 38 and 39, the combined teachings of Blayo and Abidi fail to disclose a semiconductor device wherein a structure of the base layer corresponds to one of:

a material including silicon and polysilicon, and a silicon wafer. Curran teaches providing a material of silicon and a silicon wafer. See **FIG. 1** of Curran, wherein an inductor composed of silicon and a silicon wafer is disclosed. In view of Curran, it would have been obvious to one of ordinary skill in the art to incorporate silicon into the combined teachings of Blayo and Abidi because silicon is highly useful in silicon-based solid-state electronic devices (column 7, lines 36-37).

15. Pertaining to claims 40, 41 and 42 the combined teachings of Blayo and Abidi fail to teach a silicon oxide layer and a structured surface layer including trenches that extend in depth down to the sacrificial layer wherein the trenches border a structure to be under cut, in the structured surface area. Curran teaches a silicon oxide layer and a structured surface layer including trenches that extend in depth down to the sacrificial layer wherein the trenches border a structure to be under cut. In view of Curran, it would have been obvious to one of ordinary skill in the art to teach a silicon oxide layer and a structured surface layer including trenches that extend in depth down to the sacrificial layer wherein the trenches border a structure to be under cut in the combined teachings of Blayo and Abidi because the motivation would be to make passive electronic devices that are three dimensional and functional.

Allowable Subject Matter

16. Claims 43-48 allowed.

17. The following is an examiner's statement of reasons for allowance: reasons for allowance are recited in Applicants arguments filed August 5, 2002.

18. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC